FORM PTO-1390 (REV. 5-93) U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 670-1002

U S APPLICATION NO (If known, see 37 C F R. 1 5): 09/530023

INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/GB98/03142	October 22, 1998	October 22, 1997

TITLE OF INVENTION: Field Emission Devices

APPLICANT(S) FOR DO/EO/US: Richard Allen Tuck and Peter Graham Adpar Jones

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. X This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. _ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. _ This express request to begin national examination procedures (35 U.S.C. 371(f) at any time rather than delay examination until the expiration of the applicable time limit set in 37 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. X A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. X A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. _ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. X has been transmitted by the International Bureau.
   c. _ is not required, as the application was filed in the United States Receiving Office (RO/US).

6. _ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. X Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. _ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. X have been transmitted by the International Bureau.
   c. _ have not been made; however, the time limit for making such amendments has NOT expired.
   d. _ have not been made and will not be made.

8. _ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. X An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. _ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. _ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. X An assignment document for recording A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. X A FIRST preliminary amendment.
    _ A SECOND or SUBSEQUENT preliminary amendment.

14. _ A substitute specification.

15. _ A change of power of attorney and/or address letter.

16. _ Other items or information:

416 Rec'd PCT/PTO 21 APR 2000

U.S. APPLICATION NO (If known, see 37 C.F.R. 1.50)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/530023	PCT/GB98/03142	670-1002

17. X The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National Fee 37 CFR 1.492(a)(1)-(5)): Search Report has been prepared by the EPO or JPO $840.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) . $670.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $760.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $970.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) $96.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$840	
Surcharge of **$130.00** for furnishing the oath or declaration later than _ 20 _ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	-------	

Claims	Number Filed	Number Extra	Rate		
Total Claims	15 - 20 =	0	X $18.00	0	
Independent Claims	1 - 3 =	0	X $78.00	0	
Multiple dependent claim(s) (if applicable)			+ $260.00	0	
TOTAL OF ABOVE CALCULATIONS =				840	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).				420	
SUBTOTAL =				420	
Processing fee of **$130.00** for furnishing the English translation later than _ 20 _ 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				------	
TOTAL NATIONAL FEE =				420	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				40	
TOTAL FEES ENCLOSED =				460	
				Amount to be refunded:	
				Charged	

a. X A check in the amount of $ 460 to cover the above fees is enclosed.
b. _ Please charge my Deposit Account No. 12-0913 in the amount of $__ to cover the above fees. A duplicate copy of this sheet is enclosed.
c. X The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 12-0913 . A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate lime limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:
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Docket No: 670-1002

Applicant or Patentee: Richard Allan Tuck and Peter Graham Adpar Jones
Serial or Patent No.:
Filed or Issued:
For: FIELD EMISSION DEVICES

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) and 1.27(c)) - SMALL BUSINESS CONCERN

I hereby declare that I am

[ ] the owner of the small business concern identified below:
[X] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN Printable Field Emitters Limited
ADDRESS OF CONCERN 6 Elm Grove, Hartlepool, TS26 8LZ - United Kingdom

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9(d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled FIELD EMISSION DEVICES

by inventor(s) Richard Allan Tuck and Peter Graham Adpar Jones

described in

[X] the specification filed herewith
[ ] application serial no. , filed
[ ] patent no. , issued

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e). *NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

NAME
ADDRESS
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING Richard Allan Tuck
TITLE OF PERSON OTHER THAN OWNER Director
ADDRESS OF PERSON SIGNING 34 Park Lane, Slough, SL3 7PF, Great Britain

SIGNATURE

Date 13 April 2000

670-1002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE THE APPLICATION OF)
)
Richard Allan Tuck et al.)
)
SERIAL NO.: To be Assigned)
)
FILED: Herewith)
)
FOR: Field Emission Devices)

AMENDMENT ACCOMPANYING APPLICATION

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir:

The present application is the national filing of International Application No. PCT/GB98/03142. Before calculation of the filing fee in the United States, it is requested that the application be amended as follows:

In the Claims

Amend the claims as they presently appear in the international application as follows:

Claim 4, line 1, delete "or 3"

Claims 5, 6, 7 and 8, line 1, and claim 9, line 2, delete "any of the preceding claims" and substitute - - claim 1 - -

Amend claim 10 as follows:

10. (amended) A field emission device comprising an anode having electroluminescent phosphors (613) and a [cathode according to claim 9, wherein the cathode is a] cathode array which has been manufactured by a method in accordance with claim 2 and is arranged to bombard said phosphors (613).

Claim 13, line 1, delete "11 or 12,"

Claim 14, line 1, delete "any of claims 9 to 13" and substitute - - claim 9 - -

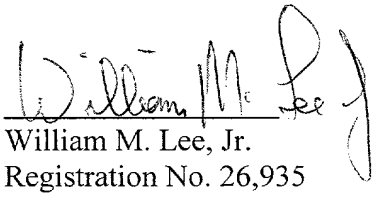
Remarks

The above amendments are being made in order to eliminate multiple dependency and improper multiple dependency before calculation of the national filing fee for the United States. Should any multiple dependency remain, that is unintended, and the Patent and Trademark Office is requested to cancel any remaining multiple dependent claims without prejudice before calculation of the filing fee in the United States.

Examination of the application on its merits is awaited.

April 21, 2000

Respectfully submitted,



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FIELD EMISSION DEVICES

This invention relates to field emission devices and in particular to methods of manufacturing addressable field electron emission cathodes. Preferred embodiments of the present invention aim to provide low manufacturing cost methods of fabricating multi-electrode control and focusing structures.

It has become clear to those skilled in the art that the keys to practical field emission devices, particularly displays, are arrangements that permit the control of the emitted current with low voltages. The majority of the art in this field relates to tip-based emitters - that is, structures that utilise atomically sharp micro-tips as the field emitting source.

There is considerable prior art relating to tip-based emitters. The main objective of workers in the art has been to place an electrode with an aperture (the gate) less than 1 μm away from each single emitting tip, so that the required high fields can by achieved using applied potentials of 100V or less - these emitters are termed gated arrays. The first practical realisation of this was described by C A Spindt, working at Stanford Research Institute in California *(J.Appl.Phys. 39,7, pp3504-3505, (1968))*. Spindt's arrays used molybdenum emitting tips which were produced, using a self masking technique, by vacuum evaporation of metal into cylindrical depressions in a SiO_2 layer on a Si substrate. Many variants and improvements on the basic Spindt technology are described in the scientific and patent literature.

An alternative important approach is the creation of gated arrays using silicon micro-engineering. Field electron emission displays utilising this

technology are being manufactured at the present time, with interest by many organisations world-wide. Again many variants have been described.

A major problem with all tip-based emitting systems is their vulnerability to damage by ion bombardment, ohmic heating at high currents and the catastrophic damage produced by electrical breakdown in the device. Making large area devices is both difficult and costly. Furthermore, in order to get low control voltages, the basic emitting element, consisting of a tip and its associated gate aperture, must be approximately one μm (one micron) or less in diameter. The creation of such structures requires semiconductor-type fabrication technology with its high associated cost structure. Moreover, when large areas are required, expensive and slow step and repeat equipment must be used.

In about 1985, it was discovered that thin films of diamond could be grown on heated substrates from a hydrogen-methane atmosphere, to provide broad area field emitters.

In 1988 S Bajic and R V Latham, *(Journal of Physics D Applied Physics, vol. 21 200-204 (1988))*, described a low-cost composite that created a high density of metal-insulator-metal-insulator-vacuum (MIMIV) emitting sites. The composite had conducting particles dispersed in an epoxy resin. The coating was applied to the surface by standard spin coating techniques.

Much later (1995) Tuck, Taylor and Latham *(GB 2304989)* improved the above MIMIV emitter by replacing the epoxy resin with an inorganic insulator that both improved stability and enabled it to be operated in sealed off vacuum devices.

The best examples of such broad-area emitters can produce usable electric currents at fields less than 10 $V\mu m^{-1}$. In the context of this specification, a broad-area field emitter is any material that by virtue of its composition, micro-structure, work function or other property emits useable electronic currents at macroscopic electrical fields that might be reasonably generated at a planar or near-planar surface - that is, without the use of atomically sharp micro-tips as emitting sites.

Electron optical analysis shows that the feature size required to control a broad-area emitter is nearly an order of magnitude larger than for a tip-based system. Zhu et al *(US Patent 5,283,501)* describes such structures with diamond-based emitters. Moyer *(US Patent 5,473,218)* claims an electron optical improvement in which a conducting layer sits upon the broad-area emitter to both prevent emission into the gate insulator and focus electrons through the gate aperture. The concept of such structures was not new and is electronoptically equivalent to arrangements that had been used in thermionic devices for many decades. For example Winsor *(US Patent 3,500,110)* described a shadow grid at cathode potential to prevent unwanted electrons intercepting a grid set at a potential positive with respect to the cathode. Somewhat later Miram *(US Patent 4,096,406)* improved upon this to produce a bonded grid structure in which the shadow grid and control grid are separated by a solid insulator and placed in contact with the cathode. Moyer's arrangement simply replaced the thermionic cathode in Miram's structure with an equivalent broad-area field emitter. However, such structures are useful, with the major challenge being methods of constructing them at low cost and over large areas. It is in this area that preferred embodiments of the present invention make a contribution to the art.

In *Hoole A C F et al "Directly patterned low voltage planar tungsten lateral field emission structures", Journal of Vacuum Science and Technology: Part B, Vol 11, No. 6, 1 November 1993, Pages 2574-2578, XP000423379*, there is disclosed a combination of low-resolution and high-resolution exposure steps. This is to overcome a problem with a high resolution device having an insufficiently small field of view. No attention or teaching is given as to the low cost fabrication of field emission cathodes having gate electrodes formed over cathode electrodes.

EP 0 795 622 A1 discloses a method for forming a field emission device. This involves vacuum deposition and is concerned with controlled ion bombardment of a precursor of a multi-phase material to form layers of different properties. It does not address the matter of forming field emission devices at low cost, and in particular, provides no teaching as to how desired accuracy of alignment can be achieved at low cost. Amongst many other things, it shows a fairly typical field emitter arrangement in which a structure that may be regarded as a gate electrode, comprising an insulating layer and a conducting layer, is disposed over a structure that may be regarded as a cathode electrode, comprising a field emitting layer between two conducting layers.

Preferred embodiments of the present invention aim to provide cost-effective field emitting structures and devices that utilise broad-area emitters. The emitter structures may be used in devices that include: field electron emission display panels; high power pulse devices such as electron MASERS and gyrotrons; crossed-field microwave tubes such as CFAs; linear beam tubes such as klystrons; flash x-ray tubes; triggered spark gaps and related devices; broad area x-ray sources for sterilisation; vacuum gauges; ion

thrusters for space vehicles; particle accelerators; lamps; ozonisers; and plasma reactors.

According to one aspect of the present invention, there is provided a method of manufacturing a field electron emission cathode having at least one cathode electrode which comprises a field emitting layer between first and second conducting layers, and at least one gate electrode which overlies said cathode electrode and comprises an insulating layer and a third conducting layer, wherein said method comprises the steps of:

a. depositing on an insulating substrate to form by low resolution means, a sequence of said first conducting layer, field emitting layer and second conducting layer to form said cathode electrode;

b. depositing on said cathode electrode to form by low resolution means, a sequence of said insulating layer and third conducting layer, to form said gate electrode;

c. coating the structure thus formed with a photoresist layer;

d. exposing said photoresist layer by high resolution means to form at least one group of emitting cells, the or each said group being located in an area of overlap between one said cathode electrode and one said gate electrode;

e. etching sequentially said third conducting layer, said insulating layer and said second conducting layer to expose said field emitting layer in said cells; and

f. removing remaining areas of said photoresist layer.

Preferably, said cathode is a cathode array, said cathode electrode and said gate electrode comprise respectively cathode addressing tracks and gate addressing tracks, which tracks are arranged in addressable rows and columns, and step d. includes forming a pattern of said groups of emitting cells.

Preferably, at least one of or all of said cathode addressing tracks address(es) a plurality of rows or columns of cells.

Each row and/or column can be thin or wide, to take in as few or as many cells as desired, depending upon the application of the cathode.

Preferably, said steps of exposing and etching include the formation of fiducial marks on the cathode array, to facilitate the subsequent alignment of the array with an anode or other component after manufacture of the array.

A method as above may comprise the step of forming at least one of said conducting layers by application of a liquid bright metal or by electroless plating.

A method as above may comprise the step of forming at least one of said conducting layers by a means other than vacuum evaporation or sputtering.

Preferably, said field emitting layer comprises a layer of broad area field emitter material.

A method as above may comprise the further steps of depositing sequentially a second insulating layer and fourth conducting layer onto the cathode after completion of steps a. to f., to form a focus grid.

The invention extends to a field electron emission cathode which has been manufactured by a method according to any of the preceding aspects of the invention.

According to another aspect of the present invention, there is provided a field emission device comprising an anode having electroluminescent phosphors and a cathode as above, wherein the cathode is a cathode array as above and is arranged to bombard said phosphors.

Preferably, said phosphors are arranged in groups of red, green and blue to form a colour display.

A field emission device as above may include anode driving means for energising said red, green and blue groups in turn.

A field emission device as above may further comprise an electrode of interdigitate or mesh form which is interposed between said phosphors and is arranged to be driven at a potential less than that at which said phosphors are driven, thereby to form potential wells around the phosphors in order to attract electrons towards said phosphors and compensate for any misalignment between cathode and anode.

The cathode may be provided with a further control grid over said gate electrode, and a driving means for so driving said control grid as to retard electrons emitted by the cathode.

Such a field emission device may further comprise means for providing a magnetic field normal to the emitter surface.

The first conducting layer, field emitting layer and second conducting layer may be patterned using low resolution means, as a whole or on a layer by layer basis. The same applies to the insulating layer and third conducting layer. The high resolution exposure step is preferably the only high resolution step required in the whole manufacturing method, and is such that the tolerance on location of the groups, with respect to intersections of the cathode and gate electrodes, is determined by the relatively large cathode and gate electrode dimensions (e.g. as tracks in rows and columns) rather than the much smaller emitter cell dimension. A first etch for the conducting layers is preferably chosen such that it does not attack the insulating or field emitting layers. A second etch for the insulating layers is preferably chosen such that it does not attack the conducting layers. Thus, the etching can be being carried out in sequential steps using the first and second etches alternately, such that each layer after etching forms a mask for the next layer to be etched, thereby providing self-alignment of the apertures in the layers.

In the context of this specification, the meaning of "low resolution means" and "high resolution means" is as follows. The high resolution means is a means capable of forming well-defined structures of the chosen emitter cell size. The low resolution means is a means capable of forming well-defined structures of the chosen size of cathode and gate electrodes but not of the smaller, chosen emitter cell size.

For example, the high resolution means may be a means capable of forming well-defined structures of a minimum size which is equal to or

smaller than 50%, 40%, 30%, 20%, 10% or 5% of the minimum size of well-defined structure that can be formed by the low resolution means. The low resolution means may be a lithographic means that can form well-defined structures down to a minimum dimension of 100, 70, 50, 40 or 30 μm. The high resolution means may be a photo-etching means that can form well-defined structures down to a minimum dimension of 20 or 10 μm or less, and preferably down to a few μm across or less. As one example, cathode and gate tracks 100 μm across are formed by lithography means, and emitter cells 8 μm across are formed by photo-etching means.

For a better understanding of the invention, and to show how embodiments of the same may be carried into effect, reference will now be made, by way of example, to the accompanying diagrammatic drawings, in which:

Figure 1a shows four pixels of an addressable array as would be used in a large area monochrome field emission display;

Figure 1b shows an idealised emitter cell structure;

Figure 1c illustrates the problems of realising such a structure using thick film fabrication techniques;

Figure 1d shows how a near-ideal emitter cell structure may be fabricated using liquid bright gold and a glaze;

Figure 1e shows how the structure in Figure 1d may be improved by the use of a planarising layer between an insulator and final conducting layer;

Figure 2 shows a pixel arrangement in a colour display;

Figure 3 shows etch steps in forming an emitting cell;

Figures 4 (a) to (f) show steps in forming an addressable array using photolithography;

Figures 5 (a) to (d) shows steps in forming an addressable array using a mixture of printing and photolithography;

Figures 6 (a) and (b) show how focusing electrodes may be incorporated into devices;

Figure 7 illustrates a complete display using methods and structures described herein; and

Figures 8 (a) and (b) show how misalignment between emitter cell groups and phosphor patches on an anode may be accommodated by special anode structures.

Embodiments of this invention may have many applications and will be described by way of the following examples. It should be understood that the following descriptions are only illustrative of certain embodiments of the invention. Various alternatives and modifications can devised by those skilled in the art.

In large field emitting displays the pixel dimensions are well within the capabilities of a number of low cost patterning techniques such as screen

printing or photo-etching. For example printed circuits can now be made with well defined 75 μm tracks.

Figure 1a shows four pixels in a hypothetical 16:9 HDTV display (monochrome for simplicity) with a diagonal dimension of one metre. Dimension 131 is 0.75 mm and dimension 130 is 0.50 mm. Figure 2 shows two pixels of a similar colour display where dimensions 234 and 235 correspond with dimensions 131 and 130 in Figure 1a. Columns 231,232 and 233 control current flow to phosphors in the three primary colours.

Referring again to Figure 1a, it can be seen that cathode address rows 112 and gate address columns 122 are some tenths of a millimetre wide and capable of being formed by a range of printing and lithographic techniques. However, the emitter cell dimensions 120 are dictated by the transconductance required to achieve the desired control voltage. Because of the large number of channels, the drive electronics form a major cost element in any matrix addressed display, with higher voltage devices costing proportionally more. To achieve overall acceptable costs the drive voltages are preferably a few tens of volts.

With reference to Figure 1a, the emitter cells may be arrays of, for example, slotted 120 or circular forms 121. Figure 1b shows a section across the narrow dimension of two such emitter cells. The structure is formed on an insulating substrate 111. The layers are as follows: cathode address rows 112; a field emitter material 113; shadow grid layer 114; gate (grid) insulator layer 115; grid address columns 116.

For electron optical reasons dimensions 118 and 119 must be comparable with each other. Such an arrangement also facilitates easy

etching. Electrostatic modelling shows that for a 40V control voltage swing (negative-going on the rows and positive-going on the columns) dimension 118 is approximately 8 μm. For a 15V swing it reduces to approximately 4 μm.

Whilst these dimensions are small, it has occurred to us that, with a suitable self-aligning process, single exposures of resist patterns to create them fall within the regime of one to one contact exposure or one to one proximity exposure with collimated illumination. Suitable large area high intensity exposure systems, both with and without collimation, are manufactured for printed circuit board fabrication. It is only if multiple exposures are required that the very expensive and slow stepping and alignment equipment that characterises semiconductor manufacture is required. Furthermore, the location of each emitter group within the pixel region may be subject to a much larger tolerance (position 141 to 140) than that required if multiple mask steps were required to form the emitter cells.

To enable the above emitter patches to be aligned with the phosphor pattern on the anode during the assembly of the display panel, fiducial marks in known positions relative to the pattern of emitter cells may be photo-etched during the single high resolution mask stage.

Given that the row and column structures are of a size capable of being screen printed one might be tempted to consider using standard electronic thick film circuit pastes to form the structures. Figure 1c illustrates the problem with this approach where the goal is a structure as in Figure 1b with dimension 118 of approximately 8 μm and dimension 119 approximately 5 μm. Conducting thick film pastes are made from metallic particles and a

glass fritt in an appropriate vehicle. Minimum layer thicknesses are around 5 μm with roughness of ±1 to 2 μm. Proprietary insulating pastes have similar roughness.

It can be seen that, even without any undercutting that may occur during etching, the structures formed by standard thick film techniques are a very poor representation of the ideal structure in Figure 1b. Not only would there be excessive variability from cell to cell but the extra depth 146 compared with the diameter 145 would be electronoptically unacceptable.

Inspection of Figure 1c shows that excessive thickness and much of the irregularity in the layers is caused by those formed from conducting pastes 142. For this reason the vast majority of field emission device fabrication processes use vacuum or plasma deposited thin films that closely conform to the profile of the substrate. Their use within examples of this invention is not precluded. However, the deposition of such films requires expensive equipment especially at large substrate sizes and high throughputs: consequently maximum reductions in manufacturing cost may only be realised using deposition techniques that do not require vacuum systems.

In a number of unrelated industries, specularly reflecting films have been produced by chemical techniques, with a good example being the silvering on mirrors. In the architectural glass industry, infrared reflecting coatings, which were produced by sputter coating, are now made by the much lower cost in situ spray pyrolysis of tin oxide films directly onto hot float glass.

For many years, the pottery and glass industries have decorated their wares with bright metallic layers using a paint that contains organometallic

compounds - the so called resinate or bright golds, palladiums and platinums. The metallic layer is formed by applying a paint and then firing the object in air at temperatures between 480°C and 920°C at which point the organometallic compound decomposes to yield pure metal films 0.1 to 0.2 µm thick. Traces of metals such as rhodium and chromium are added to control morphology and assist in adhesion. Currently most of the products and development activity concentrate on the decorative properties of the films. However, the technology is well established. Although little (or not) used, or known of, in the art today, such techniques have been used in the past by the electron tube industry. For example Fred Rosebury's classic text "Handbook of Electron Tube and Vacuum Techniques" originally published in 1964 *(Reprinted by American Institute of Physics - ISBN 1-56396-121-0)* gives a recipe for liquid bright platinum. More recently Koroda *(US Patent 4,098,939)* describes their use for the electrodes in a vacuum fluorescent display.

In critical electronic applications of liquid bright golds, care is required to avoid a bloom of sodium sulphate forming on the surface of the films. The bloom is believed to be formed by sodium compounds reacting with sulphur compounds (sulphur dioxide and/or trioxide) from the decomposition of the sulphur based gold organometallic compounds. Such bloom may be minimised or eliminated by either the use of either a low sodium glass - such as borosilicate - or by the use of coatings on sodalime glass. One suitable coating is silica deposited from a vapour phase precursor onto hot float glass. Glass treated in this way is manufactured by Pilkington under the trade name Permabloc.

Accordingly, by replacing the thick film conducting pastes with a liquid bright metal, preferably gold, one of the obstacles to a low-cost low-

voltage field emission display can be overcome. The coating formulation may be deposited by spraying, spinning, roller coating, screen printing, wire roll coating or other suitable technique and then simply fired in air. In the case of some of these techniques, for example screen printing, the formulation may be directly applied in the conducting track pattern, thus eliminating a photolithography stage.

Clearly there are other non-vacuum techniques for producing metal films. However, we are unaware of the use of any such techniques in the art of field emission devices. In part this must be due to the use of established semiconductor fabrication processes by workers who have migrated from that art. Where deviations from established techniques have taken place they are slight. For example DeMercurio et al *(US Patent 5,458,520)* uses electroplating within a gate microtip structure but only then to thicken up layers and close apertures, the initial metal layers being deposited by vacuum means.

An alternative method of forming the conducting elements is to use electroless plating with a photo-activated catalyst. There are other non-vacuum methods.

The insulating pastes used in traditional thick film technology may be replaced with a glass formulation which can be taken well past its melting point into a region where it has low viscosity and allowed to flow to a smooth film (as in a glaze) to form uniform (or near uniform) thickness gate-cathode insulator layers.

An alternative method of forming the insulating layer is by using liquid chemical precursors such as sol gels, aerogels or polysiloxanes. Once the

layer is formed it is heated to decompose the precursor to form an inorganic compound such as an oxide (e.g. Silica), a ceramic or a glass.

Figure 1d illustrates that by bringing together a low cost method of forming smooth metal layers 150 derived from a liquid bright metal, electroless plating or other suitable process and the insulator layer 151 formed from a complementary low-cost process, structures close to the ideal shown in Figure 1b may be realised.

If required, (see Figure 1e) this arrangement may be further improved by using a planarising layer 152 such as one of the spin-on glass formulations widely used in the semiconductor industry.

Example I

Referring now to Figure 3, we will describe an illustrative example. In this, emitter cells may be formed in gold/low melting point glass laminated structures on a glass substrate using wet etch processes. Naturally, dry etch processes can be used but these increase manufacturing cost.

One advantage of this combination of materials is that because low melting point glasses and gold have coefficients of thermal expansion close to that of soda lime glass, a reasonably strain free structure is produced.

Prior to stage 1, first conductive layer 301, field emitter layer 302, second conductive layer 303, insulator 304 and third, gate conductor layer 305 have been formed on substrate 300. Thus, stage 1 joins the process at a point at which all of the track patterns have been formed by low resolution patterning techniques and an appropriate photoresist layer 306 has been

exposed by high resolution means and developed with a pattern of grid cell apertures to expose these regions 307 of the laminate to various etch stages. A resist or lacquer will also have been applied to protect the reverse side and edges of the glass substrate.

The requirement is for two etch solutions. One solution must remove gold but not attack glass and the other remove glass but not attack gold. In this way, self-alignment of the cell structure is obtained, as will become apparent from the following description.

A suitable etch for glass that does not attack gold is hydrofluoric acid.

With etches for gold there are more options. Aqua regia, the classic gold etch, is an unpleasant material and, being strongly oxidising, may attack photoresists. Two practical formulations are a solution of iodine in potassium iodide or a solution of bromine in potassium bromide *(Bahl - US Patent 4,190,489)*.

Now, returning to Figure 3, in stage 2 the structure from stage 1 is exposed to the gold etch solution. It is known by those skilled in the art that there is a tendency for the gold to etch back under the resist as shown at 309, 310. Whilst an undersize aperture may be used to compensate for this effect during the etching of the top gold layer 305, this strategy cannot be used for layer 303. It is reported in the art *(US Patent 4,131,525)* that this undercutting is caused by electrochemical effects and can be suppressed by applying a bias voltage 311 to the gold layer relative to a platinum electrode 312 immersed in the etch solution. Once the upper gold layer has been removed to expose the glass surface 308, the assembly is rinsed to remove

any active gold etch. There will be a rinsing stage between each step but, for the sake of brevity, the rest of these are not described.

In stage 3, hydrofluoric acid is used to remove the glass gate-cathode insulating layer 304. By sloping the insulator away from the exiting electron beam, and thus reducing charging effects, any undercut 315 that occurs has a beneficial effect on the electronic performance of the emitting cell but creates some new problems at stage 4. However, it is known that the voltage-current characteristic of the structure is dominated by the size of the aperture 314. Furthermore, the arrangement of electrodes focuses the electrons as they leave the cathode, making it tolerant to an increase in the diameter of the emitter size over its nominal value which may have been caused by slight over-etching 317. In all cases the gold film 303 protects the emitter from any attack by the hydrofluoric acid and acts as an etch stop. This is particularly important with a glass-based emitter such as those described in Tuck et al *(GB Patent 2304989)*.

In stage 4 the gold etch is used to remove the layer 303, with the glass layer 304 and the resist layer 306 protecting the upper gold track 305. Erosion of the upper gold layer if it overhangs the cell 319 may be compensated for in the original size of the aperture in the resist. Again, biasing of the gold layer may be used to prevent undercutting.

In stage 5 the resist is removed to leave the completed structure.

Example II

Referring now to the various parts of Figure 4, in which views on the left hand side are cutaway plan views and views on the right hand side are

sectional views, it will be seen how the above self-aligning technique may be combined with low resolution optical lithography to produce the cathode plane of a matrix addressable field emission display. All drawings are simplified and relate to a single pixel and its associated connecting tracks.

Figure 4a shows a metal/glass-based field emitter/metal sandwich 403/402/401 deposited on a substrate 400 with an exposed and developed resist pattern defining the cathode address rows 404. For illustrative purposes the metal films are formed by a liquid bright gold process and emitter film from a fused glass-based layer *(GB 2304989)*. The precursor layers may have been deposited by spraying, spinning, silk screening, wire roll coating or some other coating technique. After coating with the formulations, each of the three layers will have been fired in air to form the final composition. In production this may be conveniently performed in tunnel furnaces.

Using the etches previously described, the gold and glass-based emitter layers are sequentially and selectively removed. Finally the resist layer is removed to form the structure 411 in Figure 4b.

Figure 4c shows the structure after it has been over-coated using the same techniques with a fusible glass insulating layer 421 and a gold gate layer 422. Again firing will have taken place in air. A resist pattern is formed to define a gate address column 423. A gold etch is used to remove the unwanted material. Finally the resist is stripped off to form the structure 431 in Figure 4d. The insulator layer 421 is left intact since the chemicals used to remove it would also attack the glass substrate.

A further layer of resist is now applied, patterned and developed using a single high resolution exposure system as previously described to form the emitter cell pattern and fiducial marks 432 shown in Figure 4e.

The emitter cell etching sequence illustrated in Figure 3 previously described as Example I is now used to form the completed structure with emitter cells 441 shown in Figure 4f.

Example III

Referring now to the various parts of Figure 5, it can be seen how the above self-aligned technique may be combined with low resolution direct printing techniques to produce the cathode plane of a matrix addressable field emission display. All drawings are simplified and relate to a single pixel and its associated connecting tracks. For ease of comparison with Example II the liquid bright gold/low melting point glass is used. However, photoactivated electroless nickel plating could be used to replace the gold, with nitric acid or hydrochloric acid/ferric chloride etches. In some cases a reducing atmosphere may be used during firing operations to reduce oxidation of the nickel.

Returning now to Figure 5 we continue with the example based upon liquid bright gold and low melting point glass. Figure 5a shows substrate 511, gold 503, glass-based emitter 502, gold 501 structure formed in the same way as Example II, but in this case the precursor formulations are selectively applied, for example by screen printing, to form the desired track pattern.

Figure 5b shows a fusible glass insulator 512 and gold track 513 formed as in Example II again in the desired track pattern. If desired the insulator layer may cover the entire surface 514.

A layer of resist is now applied, patterned and developed using a single high resolution exposure system, as previously described, to form the emitter cell pattern 522 and fiducial marks 523 shown in Figure 5c.

The emitter cell etching sequence illustrated in Figure 3, previously described as Example I, is now used to form the completed structure with emitter cells 530 shown in Figure 5d.

A person skilled in the art will understand from the above teachings the significant savings in manufacturing costs that can be realised by a method which utilises a sequence of in-air processes and low-cost lithography, rather than semiconductor fabrication techniques, to form a complete field emission display cathode plane.

The use of a focus grid above a gated emitter to focus the electron beam(s) has been used and was initially described by Tuck *(US Patent 4,145,635)*. Later essentially the same arrangement was utilised in a field emitting display by Palevsky et al *(US Patent 5,543,691)*. Such a structure may be fabricated in embodiments of this invention by overlaying a further layer of insulator and a further layer of metal onto the structures of Figure 4d and 5b. Said layers may be continuous or patterned to reduce inter-track capacitance or to fulfil some other function. The emitting cells with their associated focus electrodes are then etched using the techniques previously described in Example I or, if different material systems are used, their appropriate etch systems. Figure 6a shows such a completed structure in which a substrate 600 has upon it: a cathode address layer 601; a broad area emitting layer 602; a shadow grid layer 603; a gate (grid) insulator layer 604; a control gate (grid) layer 605; a focus grid insulator layer 606 and a focus

grid 607. The anode plate 610 has upon it a transparent conducting layer 611 (for example indium tin oxide) and conducting black matrix 612 to mask the space between the cathodoluminescent phosphor patches 613. A DC potential 624 positive with respect to the ground is applied to the conducting layer 611 to accelerate the electrons from the cathode plane to energies sufficient to cause cathodoluminescence from the phosphor 613.

At the cathode plane a negative voltage 620 with respect to ground selects a cathode row, and positive voltages 621 and 622 with respect to ground modulate the current flow from the cathode. Various drive schemes may be used ranging from analogue voltage control to constant voltage pulse-width modulation. A variable voltage 623 (generally negative with respect to the control gate) forms an electron lens and focuses the beamlets.

Alternatively a much coarser focus mesh system, analogous to that described by Palevsky *(US Patent 5,543,691)*, may be fabricated by directly printing a layer of insulator and conductor onto a completed gated array. Such an arrangement is shown in Figure 6b where insulator and focus grid layers are overlaid onto a gated structure 600 identical in structure to that described earlier and illustrated in Figure 1a. Again a variable potential 604 on electrode 601 is used to focus the electron beams to strike the anode plane 603.

Moving on now to Figure 7 it can be seen how a complete field emission display may be realised that utilises the methods and structures herein described.

A cathode plane formed as described earlier 701, with or without an integral focusing grid, is joined by an hermetic seal 706 to an anode plane

702. Said anode plane 702 has upon it spacers, a conducting layer, black matrix and phosphor patches in a pixel pattern 703 as previously described. To resist the pressure of the atmosphere following evacuation spacers 704 are disposed between the pixelated structure. The spacers may be of glass, ceramic or other suitable material. The hermetic seal 706 may include a pre-formed frame and may be cemented to the cathode and anode plates with a glass fritt. During the sealing process the fiducial marks 707 (formed as previously described) are used to align the pixelated structures of the cathode and anode planes. Gettering means may be incorporated into the assembly to pump residual gasses. Some ideal locations for such getters are described by Tuck et al *(GB Patent 2,306,246)*. Evacuation and bakeout of the completed structure may be via a pumping tube and oven (not shown) or by completing the sealing process in a vacuum furnace with appropriate manipulation.

The completed display is electrically driven by a cathode addressing module 710; a column address module 711 and an anode voltage power supply 712. In the event that a focus grid is used an additional focus grid supply (not shown) is provided. Additional anode switching and focusing supplies (not shown) as later described may also be provided.

A method of forming fiducial marks to assist in the alignment of the pixelated structures on the cathode and anode planes has been described earlier and illustrated in the various parts of Figures 4 and 5. However, some residual misalignment may still occur. This is particularly troublesome in colour displays where misalignment in the direction parallel with the cathode address lines 810 may result in electrons striking the wrong phosphor patch with an associated loss in colour purity.

Figure 8a illustrates one method of making a display more tolerant of misalignment. In this arrangement the conducting layer on the anode plane is in three interdigitated segments 801, 802 and 803. Each segment has phosphors of one primary colour. Said segments are driven by independent power supplies 804, 805 and 806, each of which is switched on for one third of a frame. Electrons from the cathode plane 800 are now sequentially attracted to each colour phosphor in turn and follow trajectories 807, 808 and 809. Since the other two colour phosphors are not energised they cannot luminesce and the effects of misalignment are avoided. However, because of electrical breakdown between segments, this approach can only be used in low anode voltage systems. Such an approach has been described for tip-based displays by Clerc *(US Patent 5,225,820)*.

Figure 8b illustrates an alternative arrangement in which the display is rendered tolerant of misalignment 811 by forming focusing electrons to each phosphor patch 812 by means of an electrode of interdigitate or mesh form 813 at a less positive potential 815 than the main anode supply 814. Each phosphor patch now sits within a potential well that is sufficiently attractive to electrons 816 to compensate for modest misalignment of the pixelated structures on the cathode and anode. Such an approach has been described for tip-based displays by Tsai et al *(US Patent 5,508,584)*.

Whilst some examples of the invention have been described above in the context of a matrix addressed flat panel display, the methods and structures disclosed herein may be utilised across a wide variety of devices. In particular, a non-addressed or partially addressed electron source may be constructed and incorporated into other electron devices or displays. A focus grid structure such as previously described may be used to either focus or retard emitted electrons. If used in the retarding mode, the arrangement can,

especially when combined with a magnetic field normal to the emitter surface, provide a source of low energy electrons that can substitute for a thermionic cathode in some devices.

Figure 9 shows one example of a planar non-addressed emitter structure that may be used as an electron source in a wide variety of applications.

On an electrically insulating substrate 901 there is provided a conducting layer 902 and a broad-area field emitting layer 903. A perforated focus grid layer 904 serves to guide electrons though emitter cells 907 which are formed by apertures in insulating layer 905 and gate layer 906. Such a structure may be fabricated by any of the appropriate methods described in this specification.

In this non-addressed application the electrically insulating substrate may be replaced by an electrically conducting one (e.g. a metal) and the functions of substrate 901 and conducting layer 902 combined. A metal substrate enables welding and many other standard engineering joining techniques to be used.

The current from such a structure is controlled as follows. A device incorporating the illustrated emitter structure is used in conjunction with an electron accelerating anode (not shown in Figure 9) to collect the emitted current. A DC or pulsed power supply 909 connected to points 910 and 911 is adjusted such that in the "on" condition, a suitable positive extraction field, typically ~ 10 MV m^{-1} (10 V/μm), is applied to the areas of broad-area field emitter exposed at the base of the emitter cells 907 whereas, in the "off" condition, the applied electric field is less than the threshold value for field

emission. Naturally, the applied potential may be varied to produce a pulsed or AC emission current.

Devices that can utilise this invention may include: field electron emission and other display panels; high power pulse devices such as electron MASERS and gyrotrons; crossed-field microwave tubes such as CFAs; linear beam tubes such as klystrons; flash x-ray tubes; triggered spark gaps and related devices; broad area x-ray sources for sterilisation; vacuum gauges; ion thrusters for space vehicles; lamps; particle accelerators; ozonisers; and plasma reactors.

In this specification, the verb "comprise" has its normal dictionary meaning, to denote non-exclusive inclusion. That is, use of the word "comprise" (or any of its derivatives) to include one feature or more, does not exclude the possibility of also including further features.

CLAIMS

1. A method of manufacturing a field electron emission cathode having at least one cathode electrode which comprises a field emitting layer (302) between first and second conducting layers (301, 303), and at least one gate electrode which overlies said cathode electrode and comprises an insulating layer (304) and a third conducting layer (305), characterised in that said method comprises the steps of:

   a. depositing on an insulating substrate (300) to form by low resolution means, a sequence of said first conducting layer (301), field emitting layer (302) and second conducting layer (303) to form said at least one cathode electrode;

   b. depositing on said cathode electrode to form by low resolution means, a sequence of said insulating layer (304) and third conducting layer (305), to form said at least one gate electrode;

   c. coating the structure thus formed with a photoresist layer (306);

   d. exposing said photoresist layer (306) by high resolution means to form at least one group of emitting cells, the or each said group being located in an area of overlap between one said cathode electrode and one said gate electrode;

   e. etching sequentially said third conducting layer (304), said insulating layer (304) and said second conducting layer (303) to expose said field emitting layer (302) in said cells; and

   f. removing remaining areas of said photoresist layer (306).

2. A method according to claim 1, wherein said cathode is a cathode array, said cathode electrode and said gate electrode comprise respectively cathode addressing tracks and gate addressing tracks, which tracks are

arranged in addressable rows and columns, and step d. includes forming a pattern of said groups of emitting cells.

3. A method according to claim 2, wherein at least one of or all of said cathode addressing tracks address(es) a plurality of rows or columns of cells.

4. A method according to claim 2 or 3, wherein said steps of exposing and etching include the formation of fiducial marks (432) on the cathode array, to facilitate the subsequent alignment of the array with an anode or other component after manufacture of the array.

5. A method according to any of the preceding claims, comprising the step of forming at least one of said conducting layers (301, 303, 305) by application of a liquid bright metal or by electroless plating.

6. A method according to any of the preceding claims, comprising the step of forming at least one of said conducting layers (301, 303, 305) by a means other than vacuum evaporation or sputtering.

7. A method according to any of the preceding claims, wherein said field emitting layer (302) comprises a layer of broad area field emitter material.

8. A method according to any of the preceding claims, comprising the further steps of depositing sequentially a second insulating layer (606) and fourth conducting layer (607) onto the cathode after completion of steps a. to f., to form a focus grid.

9. A field electron emission cathode which has been manufactured by a method according to any of the preceding claims.

10. A field emission device comprising an anode having electroluminescent phosphors (613) and a cathode according to claim 9, wherein the cathode is a cathode array in accordance with claim 2 and is arranged to bombard said phosphors (613).

11. A field emission device according to claim 10, wherein said phosphors (812) are arranged in groups of red, green and blue to form a colour display.

12. A field emission device according to claim 11, including anode driving means (804, 805, 806) for energising said red, green and blue groups in turn.

13. A field emission device according to claim 10, 11 or 12, further comprising an electrode (813) of interdigitate or mesh form which is interposed between said phosphors (812) and is arranged to be driven at a potential less than that at which said phosphors (812) are driven, thereby to form potential wells around the phosphors in order to attract electrons (816) towards said phosphors (812) and compensate for any misalignment between cathode and anode.

14. A field emission device according to any of claims 9 to 13, wherein said cathode is provided with a further control grid over said gate electrode, and a driving means for so driving said control grid as to retard electrons emitted by the cathode.

15. A field emission device according to claim 14, further comprising means for providing a magnetic field normal to the emitter surface.

18. A field emission device substantially as hereinbefore described with reference to Figure 6a, Figure 6b, Figure 7, Figure 8a or Figure 8b of the accompanying drawings.

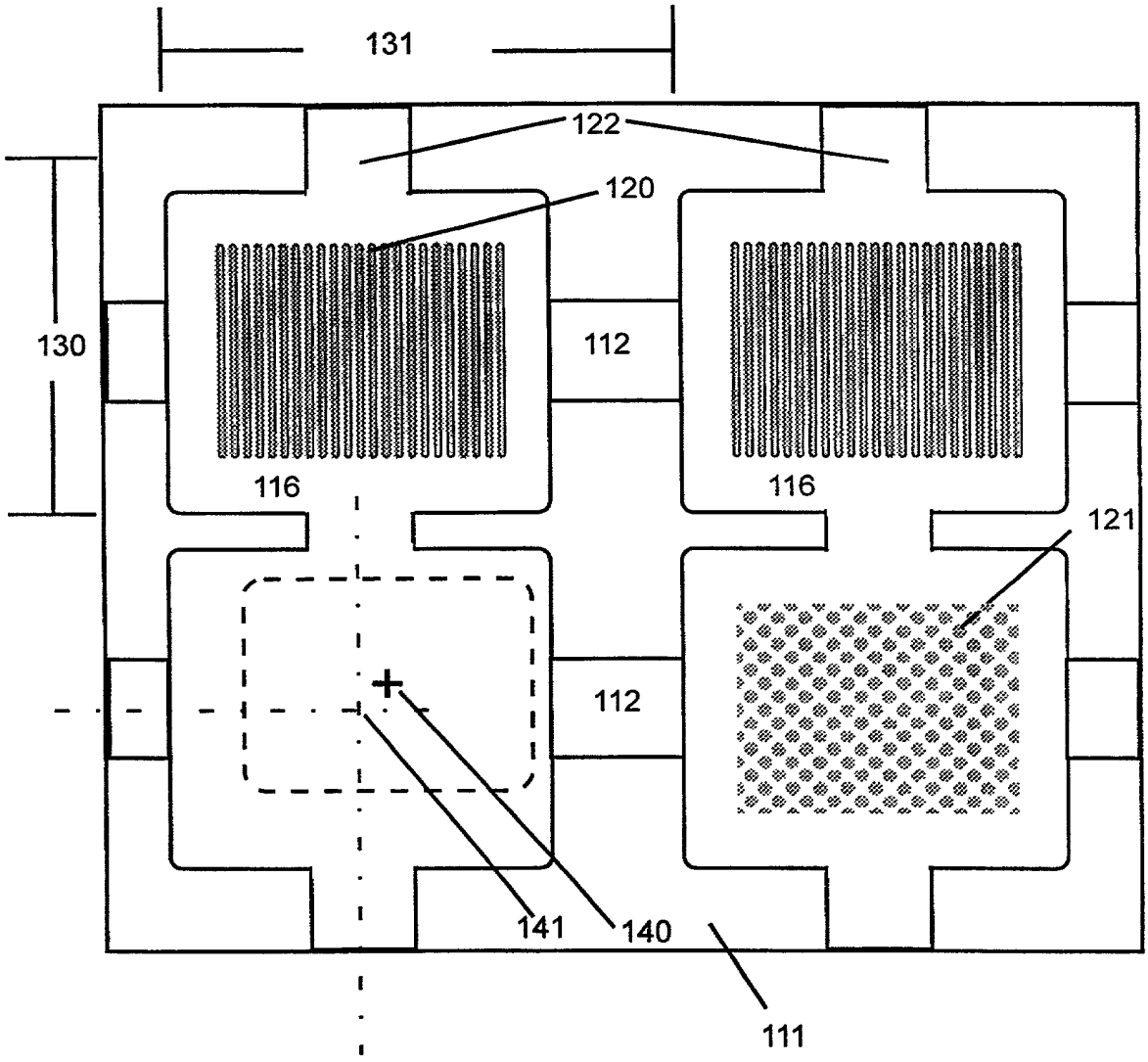


Figure 1a

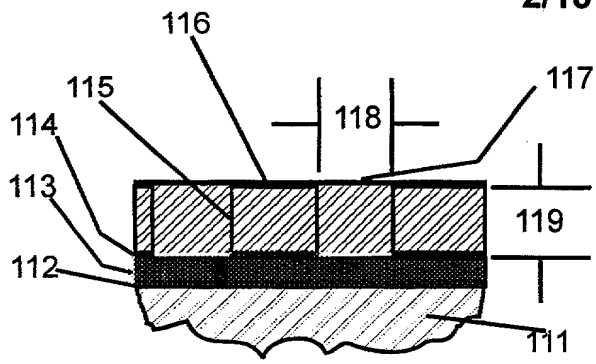


Figure 1b

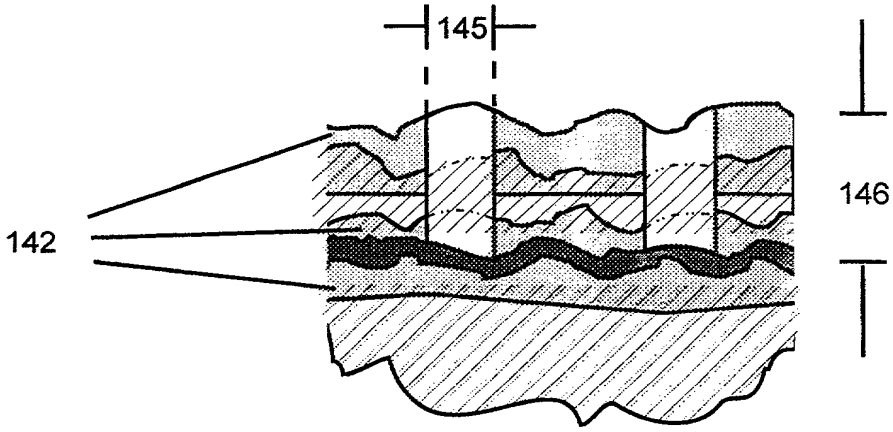


Figure 1c

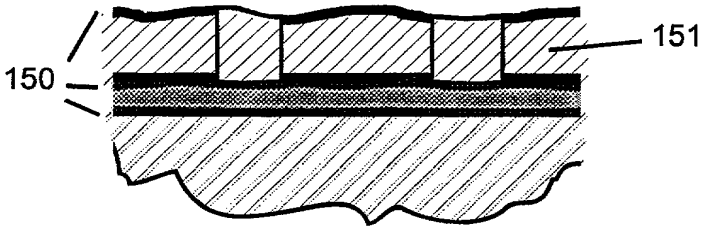


Figure 1d

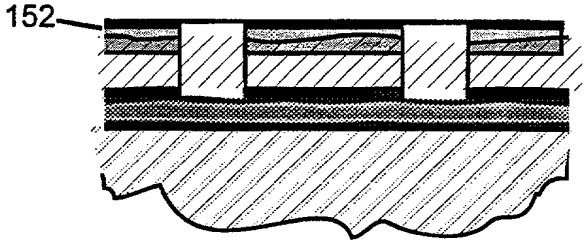


Figure 1e

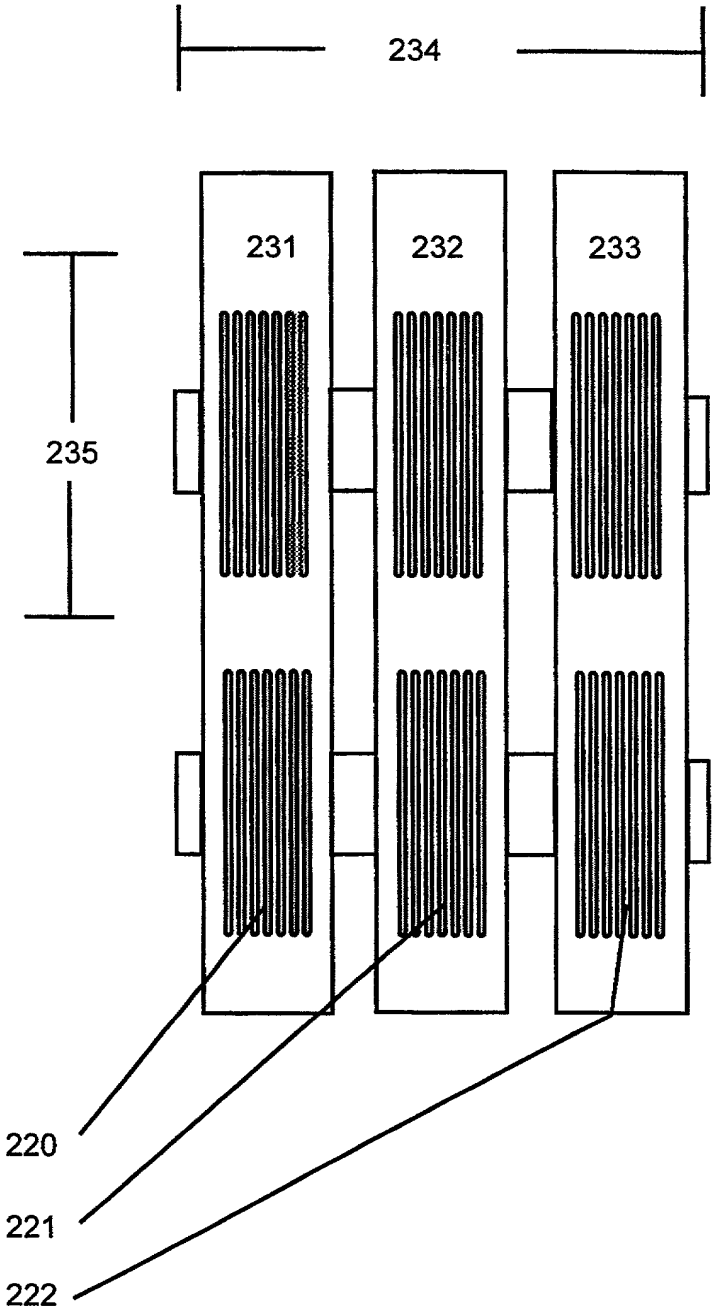
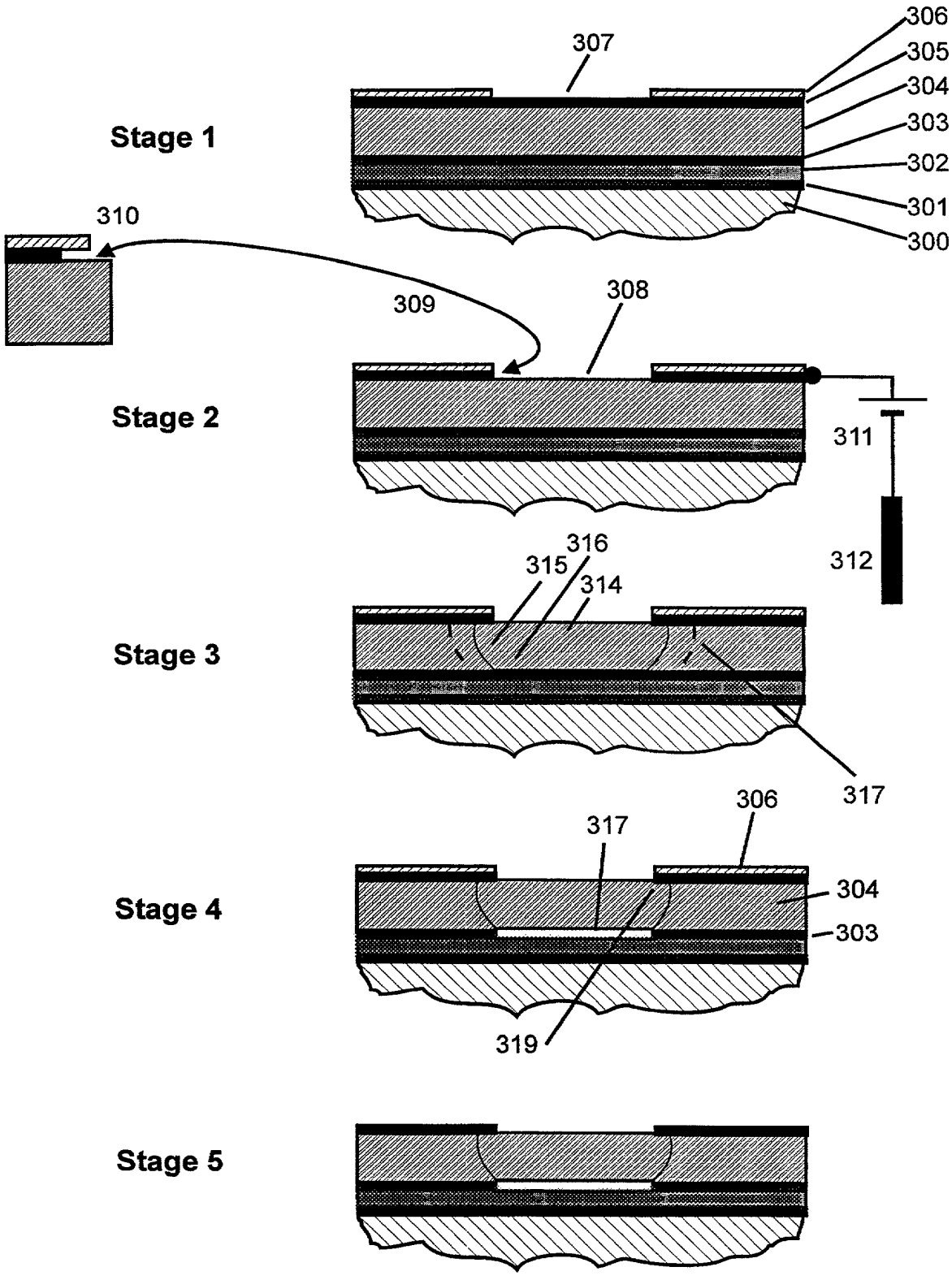


Figure 2


Stage 1
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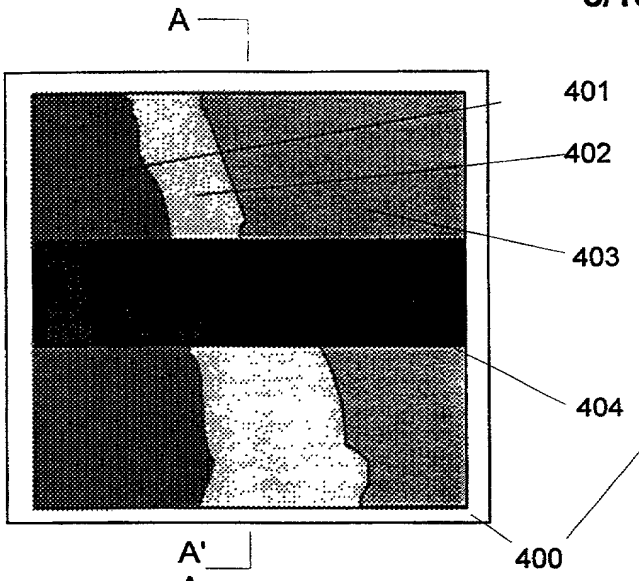
Stage 5

Figure 3



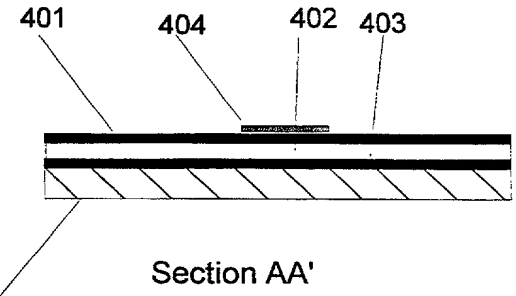
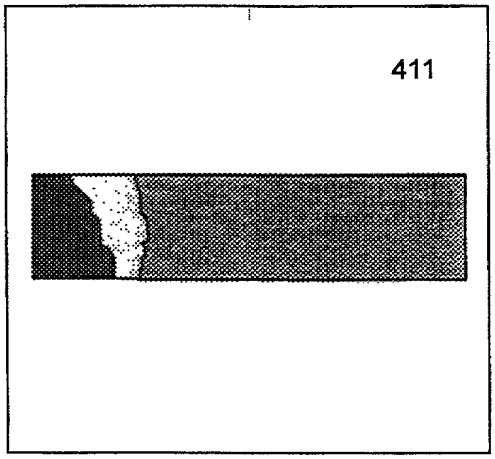


Figure 4a



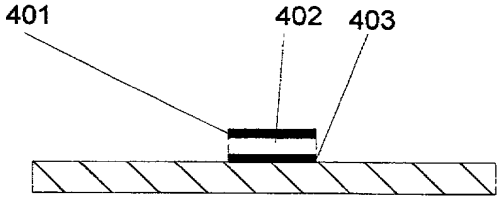
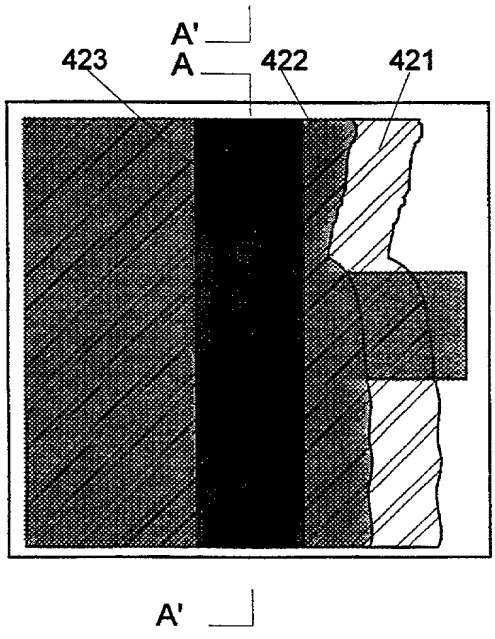


Figure 4b



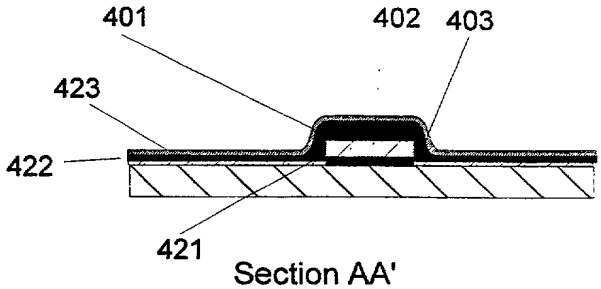


Figure 4c

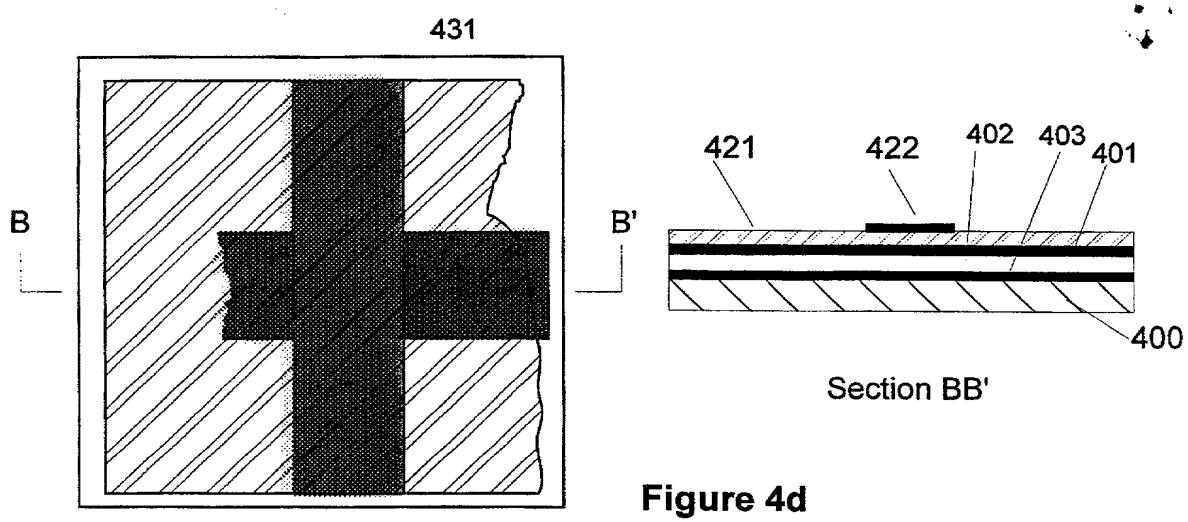


Figure 4d

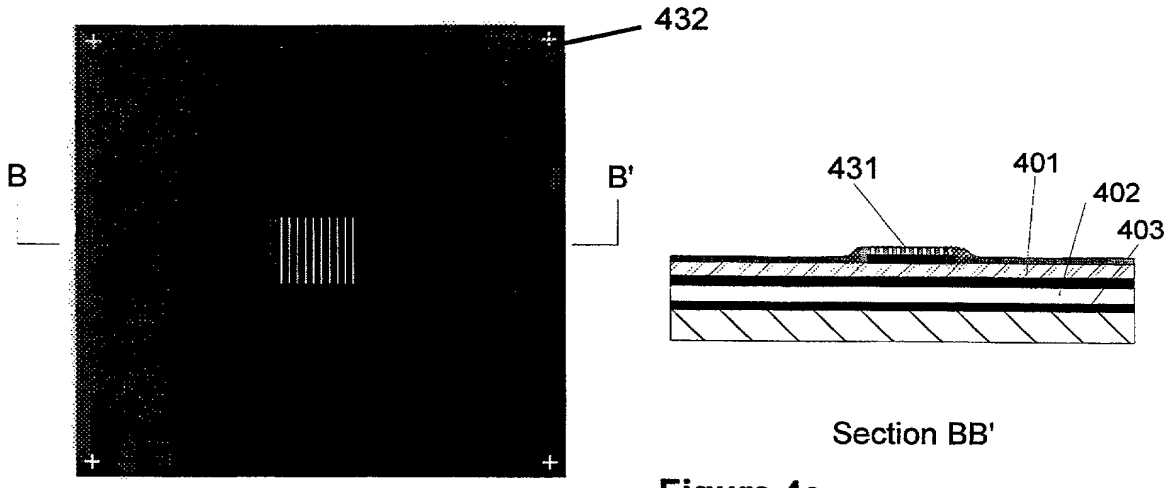


Figure 4e

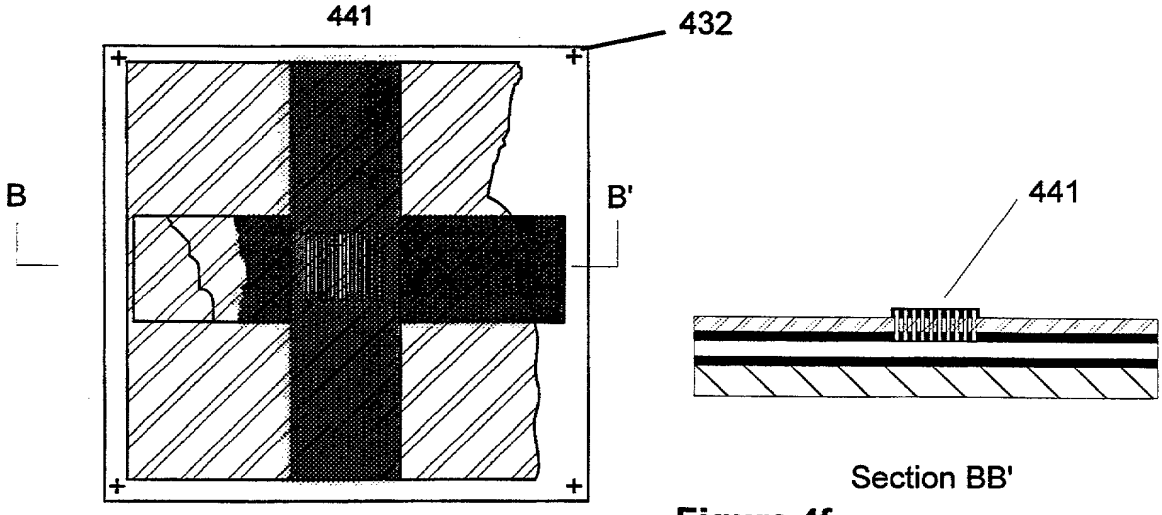
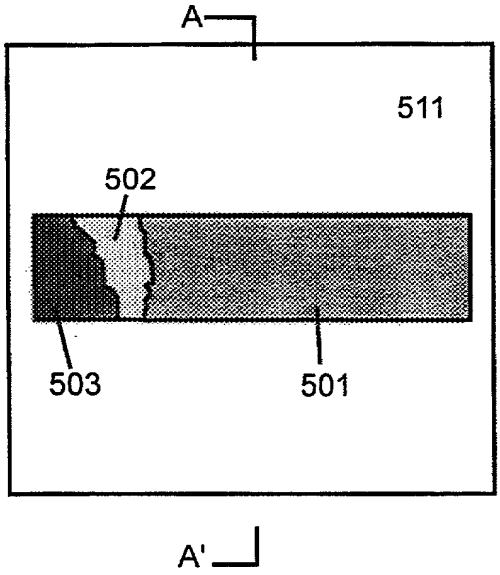
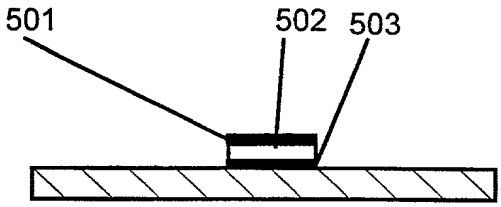


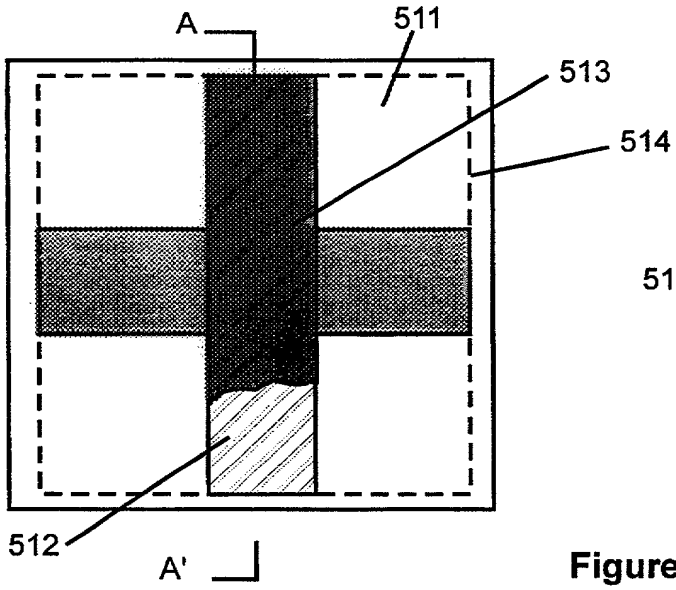
Figure 4f

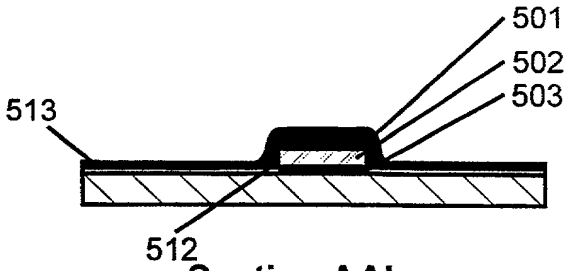




Section AA'

Figure 5a





Section AA'

Figure 5b

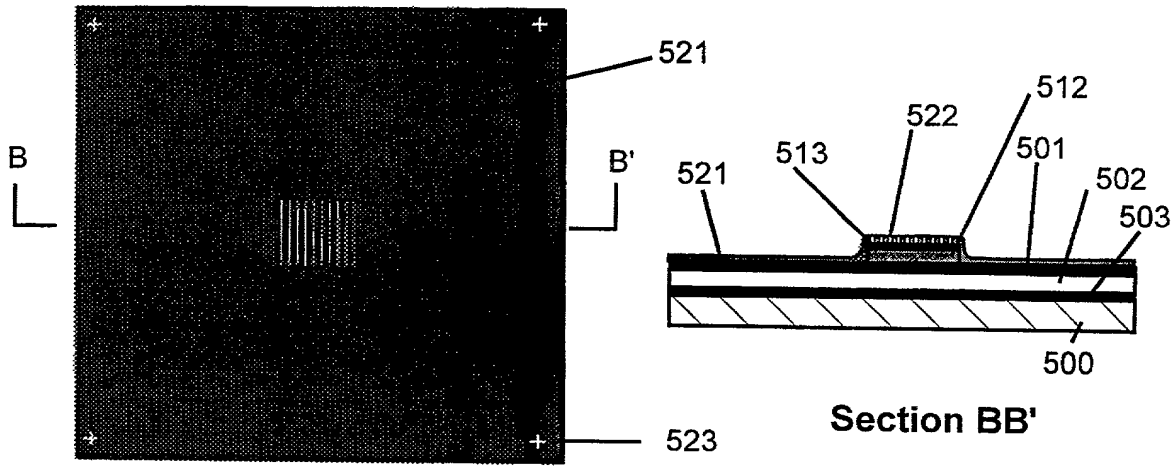


Figure 5c

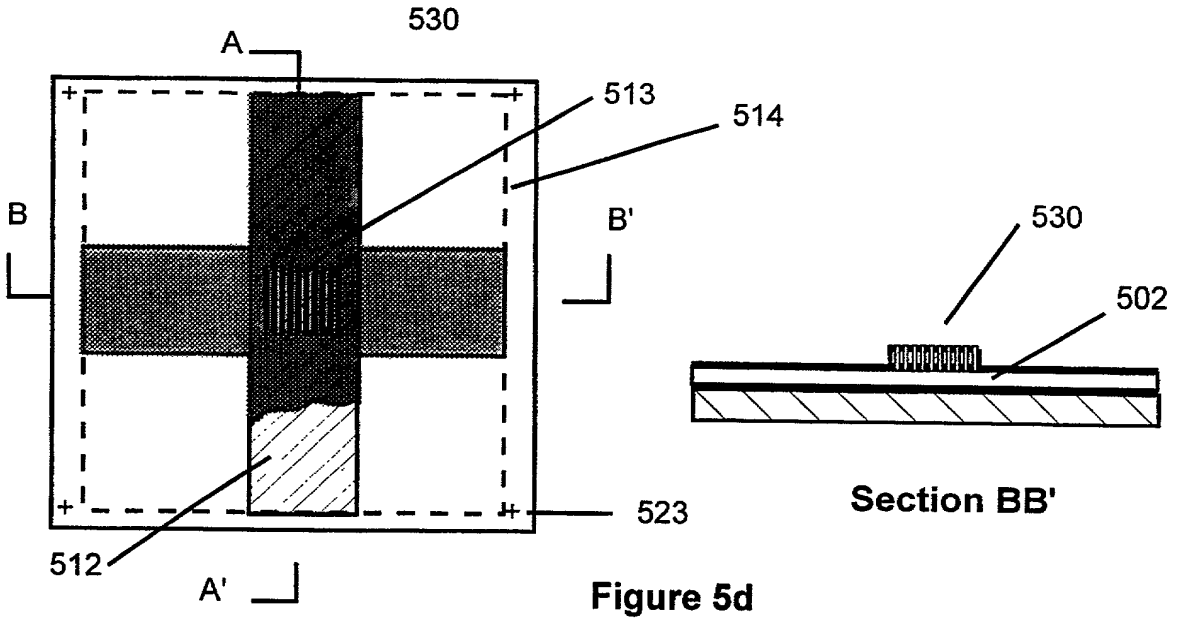
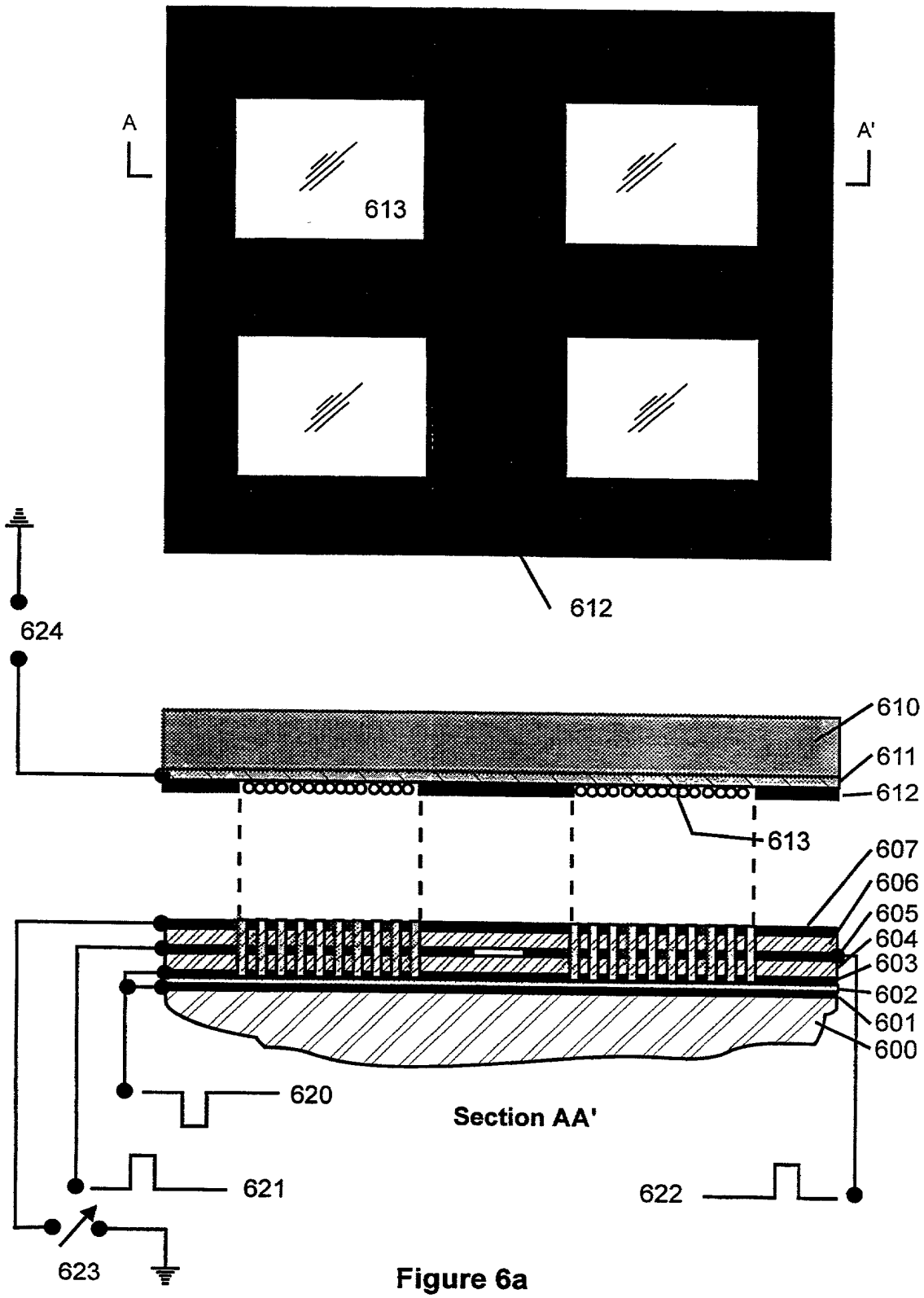


Figure 5d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Section AA'
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Figure 6a

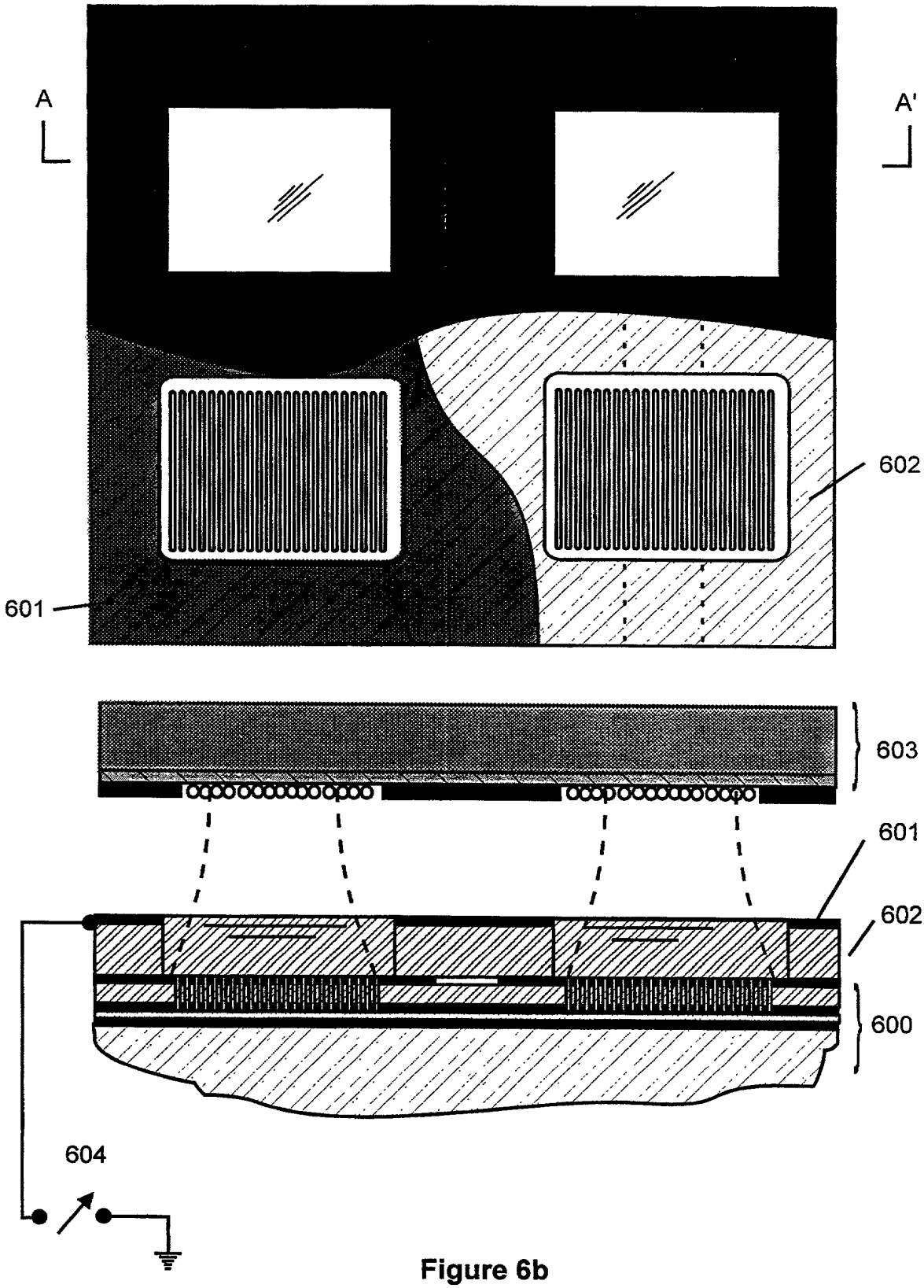

Figure 6b

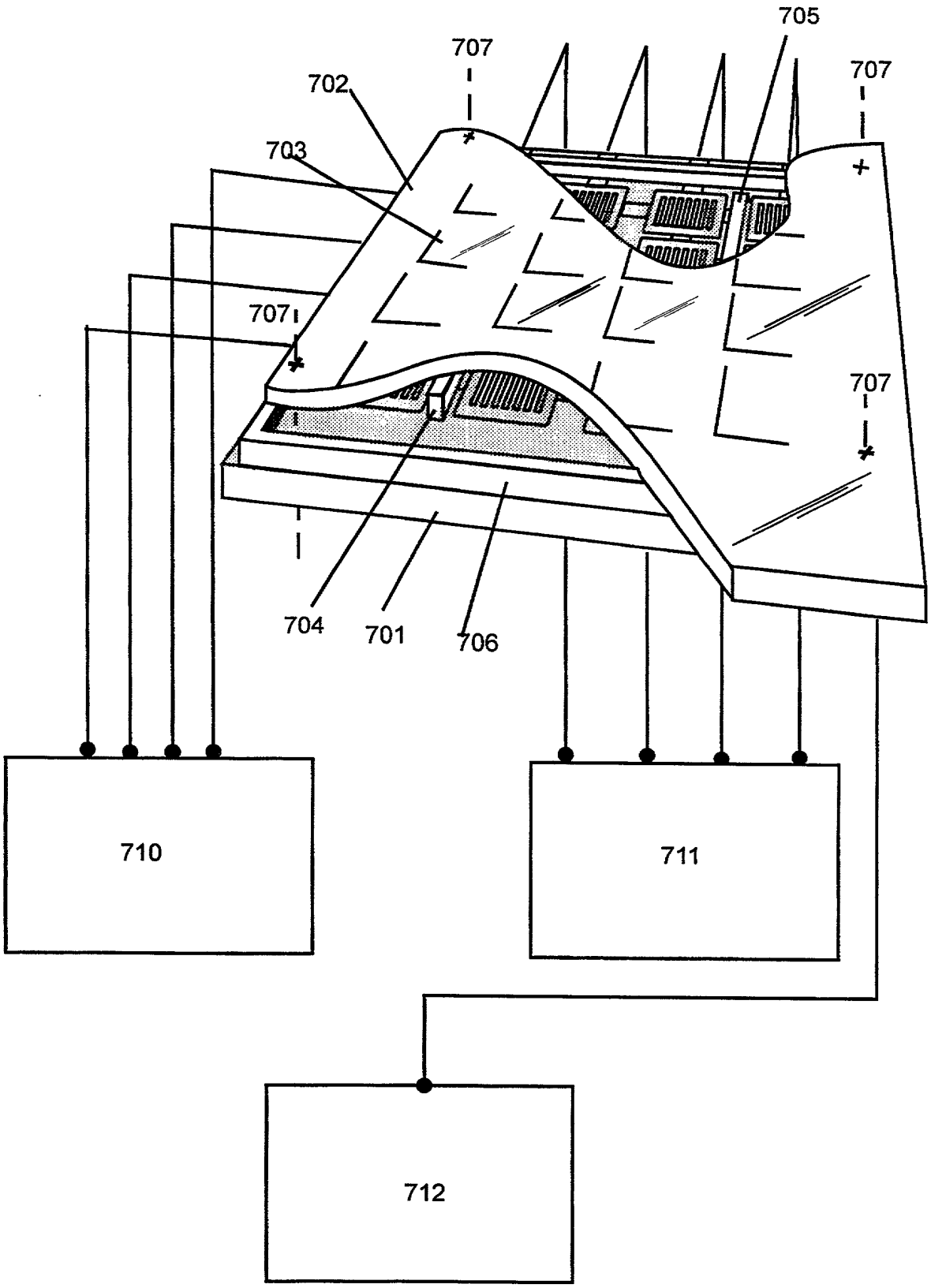

Figure 7

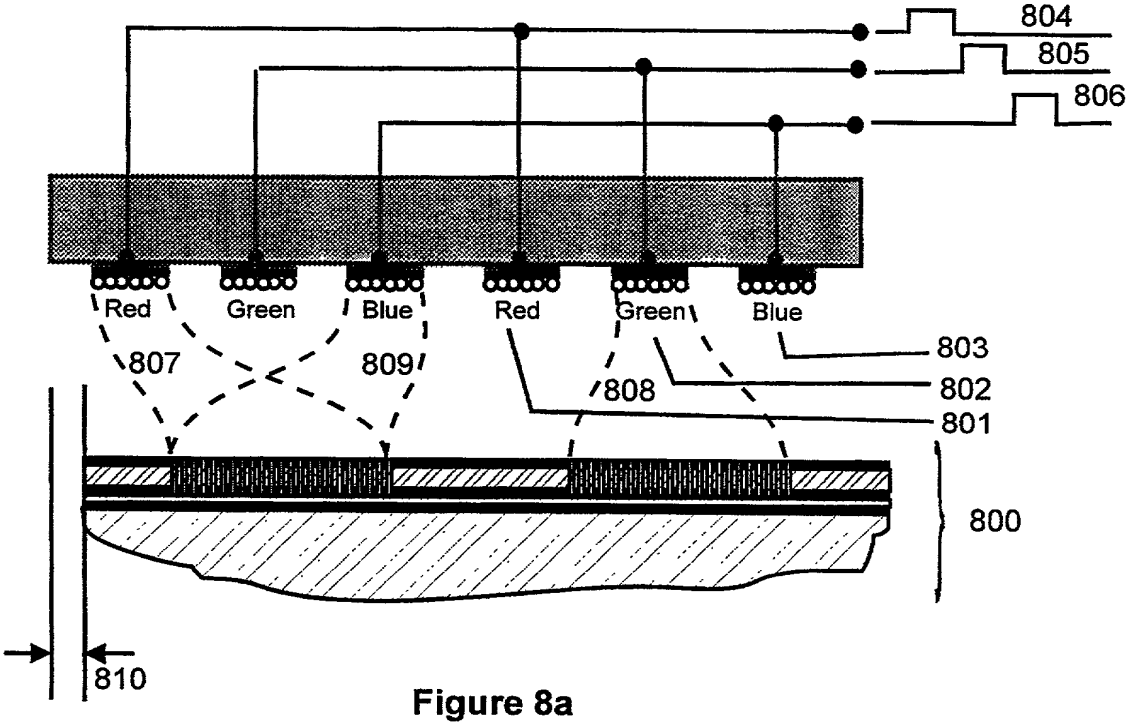

Figure 8a

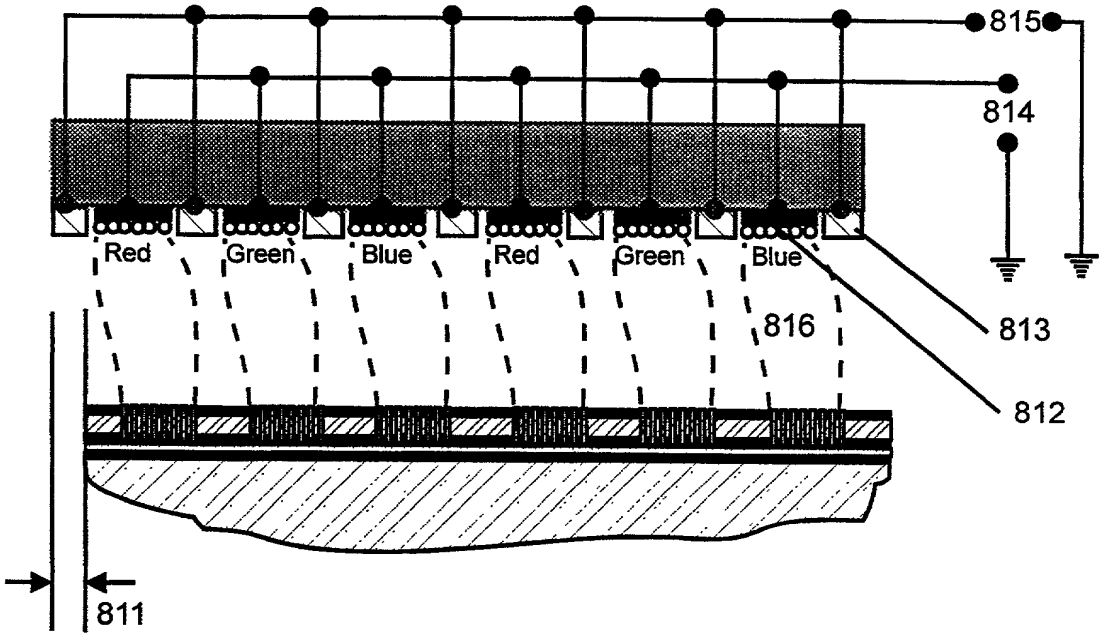

Figure 8b

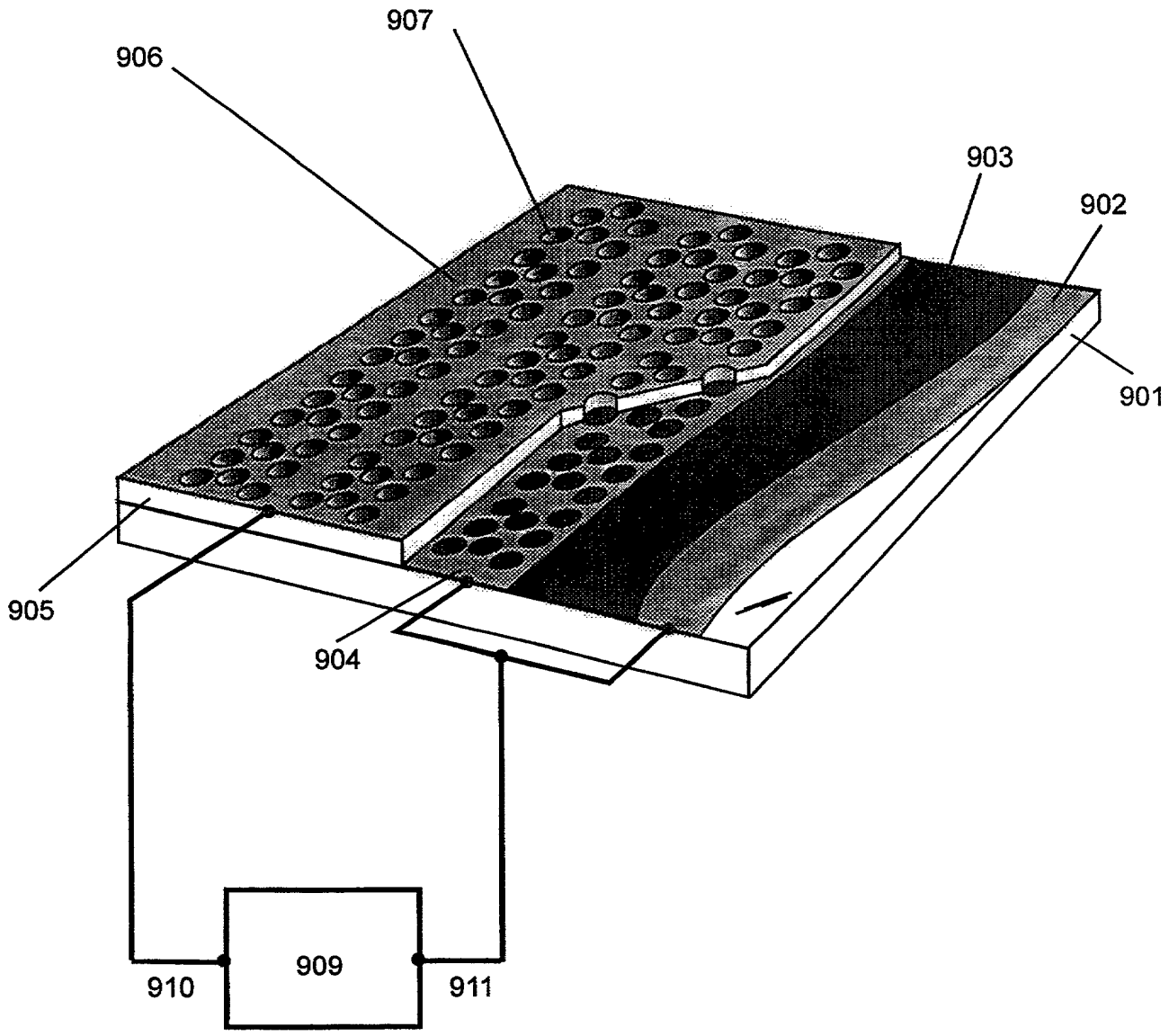

Figure 9

Attorney Docket No. 670-1002

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled FIELD EMISSION DEVICES, the specification of which:

_ is attached hereto.

X was filed on 22 October 1998 as

Application Serial No. PCT/GB98/03142 and

was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

Country	Number	Date Filed	Priority Claimed Yes	No
Great Britain	97 22258.2	22 October 1997	X	

I hereby claim the benefit under Title 35, United States Code Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

Application Serial No.	Filing Date	Status

And I hereby appoint Wm. Marshall Lee, Registration No. 16,853, John M. Mann, Registration No. 17,775, Thomas E. Smith, Registration No. 18,243, Dennis M. McWilliams, Registration No. 25,195, James R. Sweeney, Registration No. 18,721, William M. Lee, Jr., Registration No. 26,935, Glenn W. Ohlson, Registration No. 28,455, David C. Brezina, Registration No. 34,128, Jeffrey R. Gray, Registration No. 33,391, Timothy J. Engling, Registration No. 39,970, Gregory B. Beggs, Registration No. 19,286 and Gerald S. Geren, Registration No. 24,528 as my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith. It is requested that all communications be directed to Lee, Mann, Smith, McWilliams, Sweeney & Ohlson, P.O. Box 2786, Chicago, Illinois 60690-2786, telephone number (312) 368-1300.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature _____ Date 13 April 2000

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Signature _____ Date 17 April 2000.

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